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PATENT APPLICATION

PROGRAMMABLE LOGIC DEVICE HAVING NONVOLATILE MEMORY WITH USER SELECTABLE POWER CONSUMPTION

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PROGRAMMABLE LOGIC DEVICE HAVING NONVOLATILE MEMORY WITH USER SELECTABLE POWER CONSUMPTION

BACKGROUND OF THE INVENTION

[0001] The present invention relates to programmable logic devices (PLDs). In particular, the present invention relates to a nonvolatile configuration memory as part of a PLD.

[0002] FIG. 1 generally shows a PLD 100. A PLD is generally an integrated circuit device with some degree of programmability or configurability. As such, PLDs are good choices for device controllers, because they can be easily configured to operate in a wide variety of potential device environments.

[0003] The PLD 100 is exemplary of many PLDs. The PLD 100 includes an interconnect 102 and various function blocks. (The function blocks may also be referred to in the industry as IP blocks.) Exemplary function blocks include a logic block 104, a memory block 106, a digital signal processor (DSP) block 108, input/output (I/O) blocks 110, a general-purpose processor block 112, a phase-locked loop block 114, and a configuration block 116. The interconnect connects the function blocks together. Based on the intended use of the PLD, the interconnect 102 and the various function blocks may be configured in various ways.

[0004] When the PLD 100 is powered up, configuration information is transferred from a nonvolatile memory to a static random access memory (SRAM). To reduce the configuration time, it is desirable that the nonvolatile memory be able to output the configuration information at a high rate. However, when the nonvolatile memory is outputting information at a high rate, it consumes a relatively large amount of power.

[0005] Furthermore, on a PLD, space is at a premium. When space issues arise, designers must make hard decisions regarding which function blocks to eliminate or reduce in size. A memory block is one type of function block that is often chosen to be eliminated or reduced in size to overcome space issues.

[0006] There is a need for a PLD with a fast configuration time, that has a relatively larger amount of memory than certain existing PLDs, and that does not consume too much power.

BRIEF SUMMARY OF THE INVENTION

[0007] The present invention is directed toward selectable power consumption of a flash memory in a PLD.

[0008] According to one embodiment of the present invention, a programmable logic device includes a nonvolatile memory and a control circuit. The memory stores configuration information and user defined information. The memory selectively operates according to a high power state and a low power state. The control circuit controls access to the memory with a power selection signal. The high power state corresponds to accessing the memory at a high rate and the second power state corresponds to accessing the memory at a low rate. During configuration of the PLD, the control circuit controls the memory to output the configuration information at the high rate. During normal operation of the PLD, the control circuit controls the memory to selectively access the user defined information at either the high rate or at the low rate, as selected.

[0009] According to another embodiment of the present invention, a method of operating a PLD includes three steps. During configuration of the PLD, the first step is selecting a high power state and outputting configuration information from a memory at a high rate. During normal operation of the PLD, the second step is selecting a low power state for selectively accessing said memory at a low rate. Also during normal operation of the PLD, the third step is selecting the first power state for selectively accessing the memory at the high rate. (Being selectable, the second and third steps may be performed in any order.)

[0010] In this manner, configuration may be performed quickly, yet without drawing too much power during normal operation, and the effective memory size of the PLD may be increased as compared to certain other configurations.

[0011] A fuller understanding of the embodiments of the present invention may be gained from the following drawings with reference to the corresponding detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a block diagram of a programmable logic device (prior art).

[0013] FIG. 2 is a block diagram of a programmable logic device according to an embodiment of the present invention.

[0014] FIG. 3 is a flowchart of a method of operating a PLD according to an embodiment of the present invention.

[0015] FIG. 4 is a block diagram of a memory and control circuitry in the PLD of FIG. 2 according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] FIG. 2 is a block diagram of a PLD 200 according to an embodiment of the present invention. The PLD 200 includes a controller 202, a memory 204, a static RAM (SRAM) 206, and various other components 208. The various other components 208 include the interconnect, function blocks, etc. (see FIG. 1) that are otherwise present in the PLD 200.

[0017] The controller 202 controls various operations of the PLD 200. The controller 202 may be implemented as a processor that executes a control program. The control program may be software, firmware, microcode, etc. The controller 202 may also be implemented as an application specific integrated circuit.

[0018] The memory 204 stores information used by the PLD 200. Such information includes configuration information for use when the PLD 200 is being configured at power-up. The memory 204 may also be used to store information during normal operation of the PLD 200. According to the present embodiment, the memory 204 is a nonvolatile memory. That is, the memory 204 stores information even when the PLD 200 is unpowered. The memory 204 may be implemented as flash memory, electrically erasable programmable ROM (EEPROM), programmable ROM, or other types of nonvolatile memory.

[0019] The memory 204 may be selectively operated in more than one power mode. In a high power mode, the memory 204 consumes a relatively large amount of power and performs read and write operations (collectively called accesses) at a relatively high speed. In a low power mode, the memory 204 consumes a relatively small amount of power and performs accesses at a relatively low speed.

[0020] The SRAM 206 stores information used by the PLD 200. As a static RAM, though, the SRAM 206 stores information only when the PLD 200 is powered. The SRAM 206 may be located in what is termed the core of the PLD 200.

[0021] The controller 202, memory 204 and SRAM 206 have roles both during configuration and during normal operation of the PLD 200.

[0022] FIG. 3 is a flowchart of a method 300 of operating the PLD 200. In step 302, the PLD 200 is powered up and the controller 202 controls a configuration operation. During the configuration operation, the controller 202 controls the memory 204 to output the configuration information from the memory 204 to the SRAM 206. In order to reduce the amount of time spent on the configuration operation, it is desirable to access the memory 204 at high speed. High speed operation of the memory 204 corresponds to relatively high power consumption, but since many other components of the PLD 200 are not yet active, high power consumption by the memory 204 is not a concern. Once the configuration information is in the SRAM 206, the PLD 200 uses the configuration information to perform the configuration process.

[0023] In step 304, after the configuration process has been completed, the PLD 200 enters the normal operation mode. In the normal operation mode, the other components of the PLD 200 are active and drawing power. As such, the power provided to the memory 204 may be reduced.

[0024] In step 306, the user of the PLD 200 would like to access the memory 204. (The term "user" includes a person directly signaling the PLD 200, a device directly or indirectly signaling the PLD 200, the PLD 200 itself operating according to instructions programmed into the PLD 200 that control power budgets or memory access speeds, and similar means for controlling a PLD, etc.) Such access may be desired in order to use the space in the memory 204 to increase the effective memory size of the PLD 200. The user can choose to access the memory 204 at high power and high speed or at low power and low speed. Low power and low speed access may be desirable when the other components of the PLD 200 are active and drawing power, in order to maintain a given level of overall power consumption for the PLD 200.

[0025] In step 308, low power access of the memory 204 is selected, and low speed access of the memory 204 is performed. After the memory access is completed, the PLD 200 returns to normal operation (step 304).

[0026] In step 310, high power access of the memory 204 is selected, and high speed access of the memory 204 is performed. After the memory access is completed, the PLD 200 returns to normal operation (step 304).

[0027] FIG. 4 is a block diagram of a memory and control system 400 in the PLD 200 according to an embodiment of the present invention. The memory and control system 400 includes the memory 204, a high-power sense amplifier 402, a low-power sense amplifier 404, a multiplexer 406, and a NOT gate 408. A power selection signal 410 may be generated by the controller 202 or other components of the PLD 200.

[0028] The high-power sense amplifier 402 generates high speed data output from the memory 204 during high power operation (during configuration or otherwise as selected during normal operation). The low-power sense amplifier 404 generates low speed data output from the memory 204 during low power operation (as selected during normal operation).

[0029] The power selection signal 410 controls the high-power sense amplifier 402 and the low-power sense amplifier 404. When the power selection signal is at a first level, the high-power sense amplifier 402 is active and the low-power sense amplifier 404 is inactive. When the power selection signal is at a second level, the high-power sense amplifier 402 is inactive and the low-power sense amplifier 404 is active.

[0030] The power selection signal 410 also controls the multiplexer 406. When the power selection signal is at the first level, the multiplexer 406 outputs the high-speed data from the high-power sense amplifier 402. When the power selection signal is at the second level, the multiplexer 406 outputs the low-speed data from the low-power sense amplifier 402. Other similar selection circuits or devices may be used in place of the multiplexer 406 in accordance with design considerations.

[0031] Thus, the embodiments of the present invention have numerous advantages. During configuration, high power access of the memory 204 is possible because the other components of the PLD 200 are not fully active. The configuration operation may be performed with a reduced time because the memory 204 may be accessed at high speed. During normal operation, the power level of the memory 204 may be reduced. The memory 204 is still available for storage,

increasing the storage capacity of the PLD 200 compared to certain other PLDs. In addition, the memory 204 may be accessed at high speed when desired.

[0032] Although the description has mainly focused on outputting information from the memory 204, the two power modes (and corresponding speeds of operation) of the memory 204 are also applicable to inputting information to the memory 204. Outputs and inputs may both be referred to as accesses.

[0033] Although the above description has focused on specific embodiments, various modifications and their equivalents are to be considered within the scope of the present invention, which is defined by the following claims.